

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P26067PC00	FOR FURTHER ACTION	
See Form PCT/PEA/416		
International application No. PCT/ZA2004/000005	International filing date (day/month/year) 21.01.2004	Priority date (day/month/year) 21.01.2003
International Patent Classification (IPC) or national classification and IPC H01L29/78, H01L29/423, H03K17/04		
Applicant THE NORTH WEST UNIVERSITY et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

3. This report is also accompanied by ANNEXES, comprising:

- (sent to the applicant and to the International Bureau) a total of sheets, as follows:*
 - sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).*
 - sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.*
- (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s)), containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).*

4. This report contains indications relating to the following items:

- Box No. I Basis of the opinion
- Box No. II Priority
- Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- Box No. IV Lack of unity of invention
- Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- Box No. VI Certain documents cited
- Box No. VII Certain defects in the international application
- Box No. VIII Certain observations on the international application

Date of submission of the demand 26.10.2004	Date of completion of this report 28.12.2004
Name and mailing address of the International preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Lantier, R Telephone No. +49 89 2399-6081



INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/ZA2004/000005

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.
 - This report is based on translations from the original language into the following language, which is the language of a translation furnished for the purposes of:
 - international search (under Rules 12.3 and 23.1(b))
 - publication of the international application (under Rule 12.4)
 - international preliminary examination (under Rules 55.2 and/or 55.3)
2. With regard to the **elements*** of the international application, this report is based on (*replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report*):

Description, Pages

1-19 as originally filed

Claims, Numbers

1-11 as originally filed

Drawings, Sheets

1/13-13/13 as originally filed

- a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. The amendments have resulted in the cancellation of:
 - the description, pages
 - the claims, Nos.
 - the drawings, sheets/figs
 - the sequence listing (*specify*):
 - any table(s) related to sequence listing (*specify*):
4. This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
 - the description, pages
 - the claims, Nos.
 - the drawings, sheets/figs
 - the sequence listing (*specify*):
 - any table(s) related to sequence listing (*specify*):

* If item 4 applies, some or all of these sheets may be marked "superseded."

**INTERNATIONAL PRELIMINARY REPORT
ON PATENTABILITY**

International application No.
PCT/ZA2004/000005

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	5-11
	No: Claims	1-4
Inventive step (IS)	Yes: Claims	9,11
	No: Claims	5-8,10
Industrial applicability (IA)	Yes: Claims	1-11
	No: Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

**INTERNATIONAL PRELIMINARY
REPORT ON PATENTABILITY
(SEPARATE SHEET)**

International application No.
PCT/ZA2004/000005

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
D1: VISHAY DATASHEET OF N-CHANNEL 240-V MOSFETS TN2410L,
VN2406D/L, VN2410L/LS
D2: WO-A- 02/13257
D3: EP-A-1 096 573
D4: WO-A-91/11826
D5: DE-A-19905421
2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-4 is not new in the sense of Article 33(2) PCT.

Document D1 discloses a power MOSFET having very low input capacitance both in its on and in its off state. This fact is proved by the third figure on page 11-4 of the document which shows the slope of the Q-V_{gs} curves, which is inversely proportional, in first approximation, to the input capacitance. In particular, from the cited figure the slope of the curve for the disclosed device can be extrapolated before the so called 'Miller Plateau', when the device is still in its off-state, and after the 'Miller Plateau', when the V_{gs} is above the threshold voltage and an inversion layer has formed in the channel region, i.e. when the device is in its on-state. From these data a ratio C_{iss}-on/C_{iss}-off can be extracted which is below 1,5 and about 1.

Therefore, the subject-matter of claims 1, 2, 3 and 4 is not new over D1.

3. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 5, 6, 7, 8 and 10 does not involve an inventive step in the sense of Article 33(3) PCT.
- 3.1 Document D2 discloses (see fig. 5 and associated text on page 15; the references in parentheses applying to this document) a vertical power MOSFET with two control electrodes connected to two different terminals of the device, wherein the second control electrode (67,69) is superimposed on the gate (48,49) of the MOSFET with a interposed insulating layer (77,79), thus forming a capacitor. This kind of configuration has the effect, among others, of reducing also the parasitic

**INTERNATIONAL PRELIMINARY
REPORT ON PATENTABILITY
(SEPARATE SHEET)**

International application No.
PCT/ZA2004/000005

capacitances, in particular the gate-drain capacitance (see D2: page 4, lines 8-12).

The subject-matter of claims 6, 7 and 8, as far this can be understood when considered in combination with claims 5 and 10 (see item 2. under statement regarding Item VIII below) therefore differs from the device known from D2 only in that the ratio Ciss-on/Ciss-off is explicitly claimed as being below a certain value (2, 1.5 or about 1).

However, since the reduction of the gate-drain capacitance is a general goal explicitly cited by D2 and since a reduced Cgd implies also a reduction of the ratio Ciss-on/Ciss-off (see also item 1. under statement regarding Item VIII below), the person skilled in the art would always try to reach the lowest Cgd possible, thereby reducing also the ratio Ciss-on/Ciss-off and thus arriving also to values of this ratio below 2 or even around 1.

A selected range for the ratio Ciss-on/Ciss-off could only be regarded as inventive, if this selected range presents unexpected effects or properties in relation to the general goal of reducing Cgd (implying a reduction of the switching times). However, no such effects or properties are indicated in the application. Hence, no inventive step is present in the subject-matter of claims 6, 7 and 8 and also of claims 5 and 10 (Article 33(3) PCT), when considering claim 5 in light of claim 10 and thus interpreting the term "gate terminal" as simply an external terminal (see again item 2. under statement regarding Item VIII below).

Re Item VIII

Certain observations on the international application

1. Claims 1, 3, 4 do not meet the requirements of Article 6 PCT in that the matter for which protection is sought is not clearly defined. The claims attempt to define the subject-matter in terms of the result to be achieved, which merely amounts to a statement of the underlying problem, without providing the technical features necessary for achieving this result.

In particular, it is further noted that it is a general goal for power Mos devices used in high frequency application trying to reduce the gate to drain capacitance Cgd, also called 'feedback' capacitance Crss, see for example the abstracts of documents D3, D4 and D5.

**INTERNATIONAL PRELIMINARY
REPORT ON PATENTABILITY
(SEPARATE SHEET)**

International application No.

PCT/ZA2004/000005

The input capacitance, C_{iss} , is generally defined as $C_{gs}+C_{gd}$. This capacitance in the off-state is, in first approximation, dominated by C_{gs} , therefore $C_{iss-off} \sim C_{gs}$, whereas $C_{iss-on} = C_{gs}+C_{gd}$. This means that the general goal of reducing C_{gd} aimed to in the prior art always will imply also a reduction of the ratio $C_{iss-on}/C_{iss-off}$. Choosing particular ranges for this ratio does not have any other effects than further reducing the switching times, as expected and aimed to by reducing C_{gd} in the prior art.

2. The application does not meet the requirements of Article 6 PCT, because claims 5-9 and 10 (when considered as dependent on any one of claims 5, 7, 8, 9) are not clear.

Claim 10 refers to a fourth terminal of the device, to which the gate should be connected. Therefore, by operating the device, this terminal will directly control the gate and thus act as a gate terminal. On the other hand, claim 5 already refers to a "gate terminal" connected to a capacitor and thus enabled to indirectly control the gate. This inconsistency between the claims 5 and 10, both referring to a gate terminal, the one, claim 5, literally, the other, claim 10, in terms of its direct connection to the device gate, leads to doubt concerning the matter for which protection is sought. In particular, claims 5 and 10 seem to relate more to a method of using the apparatus (although not specified in a clear way) rather than clearly defining the apparatus in terms of its technical features.

The intended limitations are therefore not clear from these claims, contrary to the requirements of Article 6 PCT.

In view of the objections above, the term "gate terminal" in claim 5 was considered in the broadest way possible as simply an external terminal in the previous discussion on the inventive steps of claim 5-8, and 10.